REMARKS

The Examiner's Action mailed on October 5, 2009, has been received and its contents carefully considered. Additionally attached to this Amendment is a Petition for a Two-month Extension of Time, extending the period for response to March 5, 2010.

In this Amendment, Applicants have amended claim 1, and newly added claims 8-15. Claim 1 is the sole independent claim, and claims 1, 2, 4, 6 and 7-15 are pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Claims 1, 2, 4, 6 and 7 were rejected under 35 USC §112, ¶2 as indefinite. This rejection is respectfully traversed.

Regarding claim 1, the *apparent* size of the opening formed in the insulating film and the apparent size of the semiconductor chip would vary depending upon the viewing direction.

Similarly, in claim 6, the *apparent* distance between the outer periphery of the semiconductor chip and the edge of the opening of the insulating film would vary depending on the viewing direction.

Hence, the occurrences of "when the surface of the solid state device facing the semiconductor chip is viewed from vertically above" in claims 1 and 6 are not indefinite, but instead define the viewing direction for the respective

comparisons of size and distance, and it is clear that the respective features preceding this phrase are part of the claimed subject matter.

Claims 1 and 6, and claims 2, 4 and 7 that depend therefrom, are therefore definite.

Claims 1, 2, 4 and 7 were rejected under 35 USC §103(a) as obvious over *Sunohara* (US 2005/0067715 A1) in view of *Toyosawa* (US 2004/0108594 A1). This rejection is respectfully traversed.

Claim 1 recites "an insulating film provided on the surface of the solid state device facing the semiconductor chip, the insulating film having an opening greater in size than the semiconductor chip", and has been further amended to recite "wherein a difference in level caused by the opening is not located in a gap between the solid state device and the semiconductor chip".

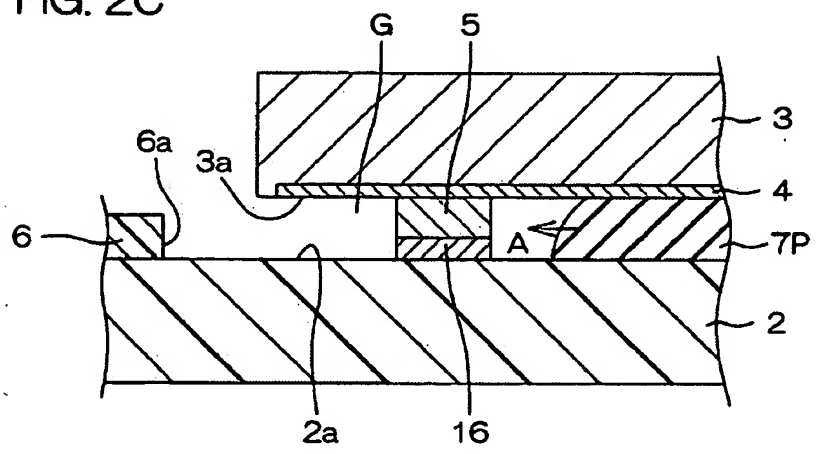
This is supported by ¶[0010] in the original specification as filed, which reads as follows:

> **[0001]** According to this invention, *the opening of the insulating film is formed to be greater in size than the semiconductor chip* when the surface of the solid state device facing the semiconductor chip is vertically viewed down in plane. *In other words, the opening of the insulating film is formed such that the semiconductor chip completely falls within the opening* when the surface of the solid state device facing the semiconductor chip is vertically viewed down in plane. Therefore, *a level difference caused by the opening of the insulating film can be prevented from locating in a gap between the solid state device and the semiconductor chip*, and a space over the periphery of the opening can be prevented from being restricted by the semiconductor chip.
>
> (*emphasis added*)

In the non-limiting example of FIG. 2C, as reproduced below, opening **6a** is greater in size than the size of the semiconductor chip **3** when viewed from above, such that the change in level between the solder resist film **6** and the wiring board **2** is not located in the gap **G** between the semiconductor chip **3** and the wiring board **2**.

ANNOTATED DRAWING

FIG. 2C

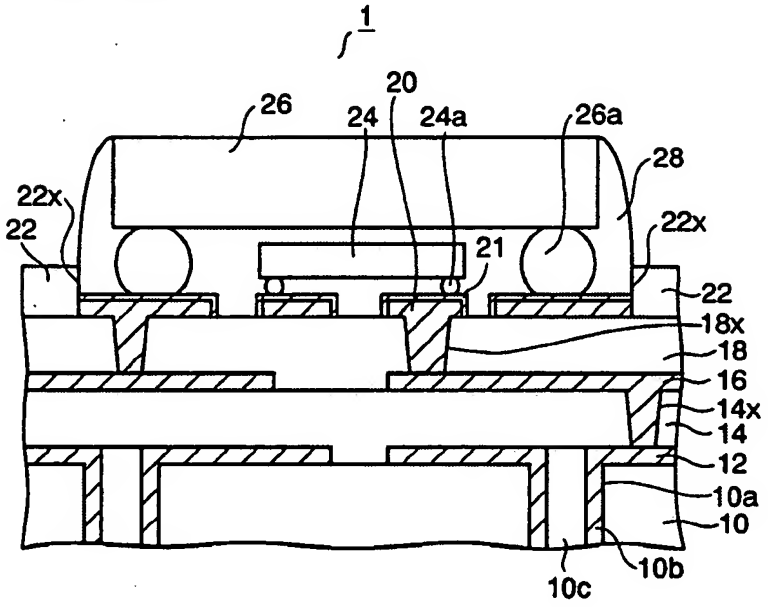


However, neither *Sunohara* nor *Toyosawa* include any teaching or suggestion of an opening that has a greater width than that of the semiconductor chip when seen from above, or when seen from more than one direction. FIG. 3H of *Sunohara* and FIG. 2(b) of *Toyosawa* both show only side views in cross section, i.e. views similar to the above FIG. 2C of the present invention:

ANNOTATED DRAWINGS

Sunohara

FIG. 3H



Toyosawa

FIG. 2 (b)

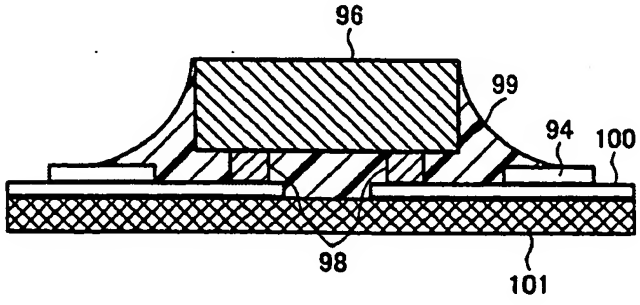


FIG. 3H of *Sunohara* shows an opening portion **22x** in solder resist film **22** that is wider than either the width of the first semiconductor chip **24** or the width of the second semiconductor chip **26**, but only when viewed from a particular side. Similarly, FIG. 2(b) of *Toyosawa* shows a space in solder resist **94** that is wider than semiconductor chip **96**, but again, only when viewed from a particular side. Nothing in either reference discloses that this is also true when viewed from other directions or from above.

Thus neither reference discloses "an insulating film provided on the surface of the solid state device facing the semiconductor chip, *the insulating film having an opening greater in size than the semiconductor chip when the surface of the solid state device facing the semiconductor chip is viewed from vertically above*" or that the semiconductor chip does not overlap the insulating film in any portion, such that "a difference in level caused by the opening in the insulating film is not located in a gap between the solid state device and the semiconductor chip", as now further recited in claim 1.

By employing such a feature, a void can be prevented from being generated when a gap between the solid state device and the semiconductor chip is filled with the liquid sealing resin. For example, see ¶[0011] in the original specification as filed, which reads as follows:

> **[0002]** Therefore, in a step of producing this semiconductor device, a void can be prevented from being generated that results from taking air into a liquid sealing resin when a gap between the solid state device and the semiconductor chip is

filled with the liquid sealing resin in order to form the sealing layer after forming the insulating film and bonding the solid state device and the semiconductor chip together. As a result, the reliability of the semiconductor device can be improved.

Thus, neither *Sunohara* nor *Toyosawa*, whether taken separately or in combination, teach or suggest either "an insulating film provided on the surface of the solid state device facing the semiconductor chip, *the insulating film having an opening greater in size than the semiconductor chip when the surface of the solid state device facing the semiconductor chip is viewed from vertically above*" or "wherein a difference in level caused by the opening is not located in a gap between the solid state device and the semiconductor chip", as recited in amended claim 1.

Consequently, claim 1 patentably defines over *Sunohara* and *Toyosawa*, and is allowable, together with claims 2, 4 and 7 that depend therefrom.

Claim 6 was rejected under 35 USC §103(a) as obvious over *Sunohara* in view of *Toyosawa* and further in view of *Urasaki et al.* (US 6,281,450 B1). This rejection is respectfully traversed.

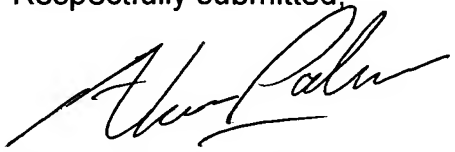
Claim 6 depends from claim 1, and as *Urasaki et al.* fails to overcome the deficiencies of *Sunohara* and *Toyosawa* with respect to claim 1, therefore claim 6 is allowable for at least the same reasons as claim 1 is allowable.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Should the remittance be accidentally missing or insufficient, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,



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Date

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ALP/pq